COMPARISON OF Si, GaAs, SiC AND GaN FET-TYPE SWITCHES FOR PULSED POWER APPLICATIONS *

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Abstract

Among the present limitations on the peak voltage of traditional Si-MOSFET switches are fundamental materials properties that are related both to intrinsic properties (such as bandgap), and to defects. Switches fabricated from semiconductors such as GaAs, SiC and GaN hold promise if hold-off voltages of several kilovolts and fast rise rates are needed. High power and short pulse (< 1 μs) applications require both fast switching speed and great current handling capability. The question arises whether any single material has all of these desired properties or whether there are intrinsic limitations. In order to investigate this, we have performed simulations of the electrical properties of FET-type switches fabricated from each of these materials. Both perfect material properties and the effects of defects have been included. The simulation results show that deep level defects degrade the device performance. Based on our simulations and on the available data, in the near term, 4H-SiC is the most attractive of the four materials for pulsed power applications.

I. INTRODUCTION

With increasing demands on the switching and on-state performance of semiconductor switches in fast pulsed power applications, wider band gap materials have been developed as possible replacements for Si. For example, GaAs Field-Effect Transistors (FET's) have been considered for such applications. Although GaAs has a direct bandgap and high electron mobility, its lack of a suitable oxide and its degraded electronic properties under high electric fields (> 4 kV/cm) limit its applications in FET's. Recently, SiC and GaN FET's have attracted interest for reasons that include their wide band gaps (> 2eV). Two figures of merit, **JM** $(E_c v_{sat}/\pi)^2$ and **BM** $(\varepsilon\mu E_c^3)$ are usually used to evaluate power device performance [1]. For GaN, the **JM** and **BM** values are comparable to those for SiC, and much higher than for Si and GaAs [2].

In addition to promising materials properties, the effect of defects must be considered when evaluating materials for pulsed power applications because they are responsible for device limitations that are not apparent based on analysis of only intrinsic properties. In this paper, we present the results of simulations of the electrical properties of a Si MOSFET and of FET's based on GaAs, 4H-SiC and Wurtzite GaN. We also compare these four materials for pulsed power applications. Major defects in these materials are included in the simulations. By this means, the influence of defects on the electrical properties can be studied.

II. SIMULATION SET UP

A. Physical Models for the Simulations

A two-dimensional simulator, ATLAS® was utilized [3]. To obtain realistic results, one must use proper microscopic models as input into the simulations. Because of the lack of parameter values in ATLAS® for some materials, it was necessary to first generate a set of such parameters by fitting experimental data available in the literature [4][5]. In our simulations, we have used physical models for the mobility, impact ionization, Shockley-Read-Hall (SRH) recombination and Auger recombination.

Effects of lattice temperature were included by adding a heat-flow equation in the simulations and by including the thermoelectric factor in the current density equations. In the simulations, the electrode drain was defined as a thermal contact with constant temperature 300K.

B. Device Structure and Defect Parameters

Because of its high current handling capability and large hold-off voltage, a buried gate Junction Field-Effect Transistor (JFET) was chosen as the basic structure for the simulations [6]. The device dimensions are given in reference [18] and optimizing of device dimensions will be discussed in a separate paper. This is shown schematically in Figure 1. The Si MOSFET doping concentrations and device dimensions used are listed in Ref. [7], except that our drift region is 20μm thick. For the other materials, we assumed that the n+ and p+ layers have the same doping concentration, 5×10^{18} cm^{-3}. The

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Table 1. Trap parameters

	EL2	N implanted[11]	i center[12]	DLN1[13]	DLN3[13]
Trap type	Acceptor	Donor	Donor	Acceptor	Acceptor
ΔE (eV)	0.688 [8]	0.51	0.53	0.25	0.59
Density (cm^{-3})	1×10^{14}[9]	3×10^{15}	1×10^{15}	1.7×10^{14}	3.3×10^{15}
σ_n (cm^2)	8×10^{-14}[8]	-	-	5×10^{-15}	1×10^{-14}
σ_p (cm^2)	2×10^{-16}[8]	6.4×10^{-15}	2×10^{-15}	-	-
g	0.84[10]	1	1	1	1

uniform doping of the n- layer is chosen 5×10^{14} cm^{-3} for the GaAs and SiC JFET's, and $5\times10^{16}cm^{-3}$ for the GaN device.

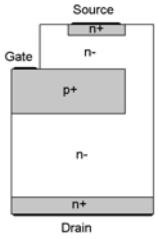

Figure 1. Cross section of vertical JFET structure.

Deep level defects can introduce energy levels near mid-gap, and can act as carrier traps and scattering centers. In GaAs, EL2 was assumed to be uniformly distributed in the n- drift region. For SiC, micropipes of wafers may have a large impact on device properties, but will not affect the results of the single cell simulations discussed here. For the SiC-based JFET, our simulations include deep levels introduced by N implantation and by *i-centers* from Al implantation along the junction interfaces. In unintentionally doped GaN with carrier concentration of 5×10^{16} cm^{-3}, DLN1 and DLN3 are the major deep level defects. The parameters associated with each of these defects are listed in Table 1. In the Si MOSFET simulation, a perfect Si material was assumed.

III. EFFECTS OF DEFECTS

As shown in Figures 2 and 3, our simulation results show that the presence of defects results in lower hold-off voltages for GaAs, GaN and 4H-SiC JFET's, as well as smaller conduction current densities in GaAs, GaN JFET's. In the following we detail these results.

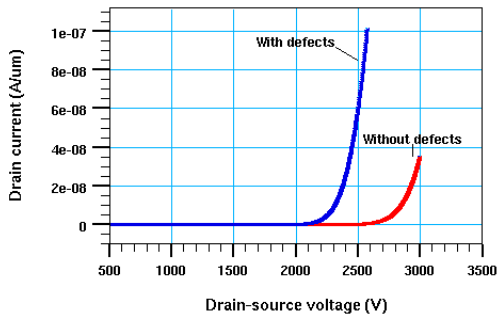

Figure 2. Predicted hold-off voltage for the 4H-SiC JFET.

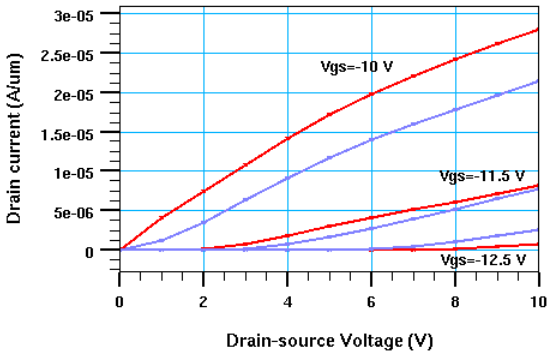

Figure 3. Predicted I - V curves for the GaN JFET. The dark curves are results for perfect GaN. The gray curves are for GaN with defects.

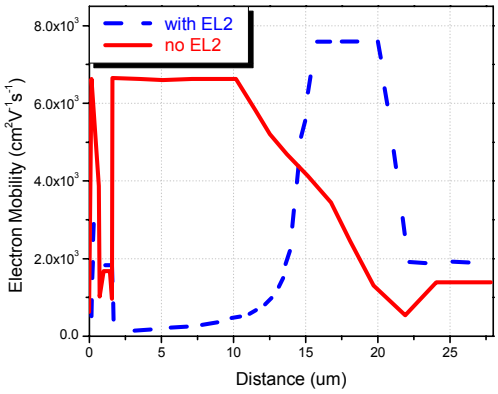

Figure 4. Predicted electron density in the GaAs vertical JFET at Vds = 300 V with and without the EL2 defect. The x-axis is the distance from the source toward the drain.

A. GaAs

EL2 is the most widely studied deep defect in GaAs, primarily because semi-insulating GaAs can be obtained by compensating EL2 with carbon or chromium. It remains thermally stable up to 1200 °C and its density is difficult to reduce [14]. In pulsed power applications, semiconductor switches are required to operate under high fields and to handle large current densities. McGregor et al. have shown that electron capture by EL2 centers is enhanced as electric field increases [15]. Figure 4 shows our results for a profile of the electron mobility in the device when it is in the off state under a drain source

voltage of 300V. The results with and without the EL2 defect are shown for comparison. Near the interface between the n+ drain and the n- drift region, most EL2 traps have been filled by electrons diffused from the highly doped drain region.

B. Wurtzite GaN

In Wurtzite GaN, the defects DLN1 and DLN3 are electron traps mostly found in thick (>10 μm) layers [12]. The formation mechanism is presently unknown. Figure 5 shows our simulation results for the electron mobility profile in the GaN device with and without these defects. Clearly, the mobility is reduced due to defect trapping and scattering. Dislocations are also a major defect in GaN. However, there is evidence that dislocations lines are parallel to the crystalline c-axis of Wurtzite GaN [16]. Thus, for the vertical device considered here, dislocations were not included in the simulations.

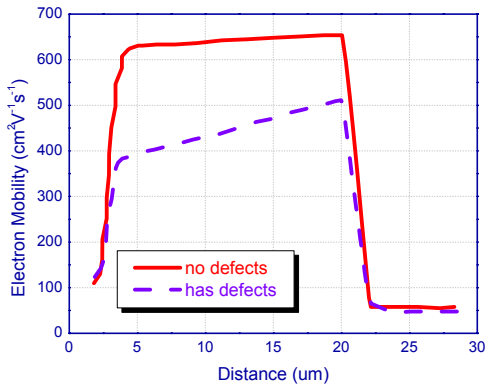

Figure 5. Predicted electron mobility in the GaN vertical JFET. The x-axis is the distance from the source toward the drain.

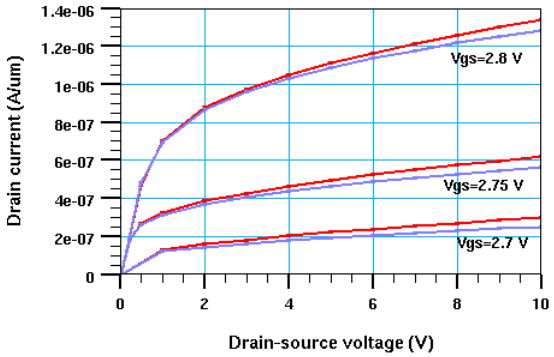

Figure 6. Predicted I-V curve for the 4H-SiC vertical JFET. The gray curves are results for the perfect material. The dark curves include the effects of defects.

C. 4H-SiC

In 4H-SiC, N and Al implantation are commonly used because these atoms have fairly high solubility and the lowest ionization energies of all impurities [11]. Since these defects are donor-like hole traps, they cause the recombination rate to decrease, so that, as a majority carrier device, the conduction current density in a 4H-SiC JFET increases. This is in agreement with our simulations. Our results are shown in Figure 6, which plots the I-V characteristics of this device. On the other hand, *i-centers* along the p-n junction cause the depletion region to shrink and lower the hold-off voltage, as is shown in Figure 2.

IV. COMPARISON OF MATERIALS

Switches based on advanced materials have promising performance which is superior to Si-based switches. In the previous section, it was shown that the presence of defects has an effect on the electrical characteristics of devices. Thus, the effects of defects must be included when making comparisons between materials for pulsed power applications.

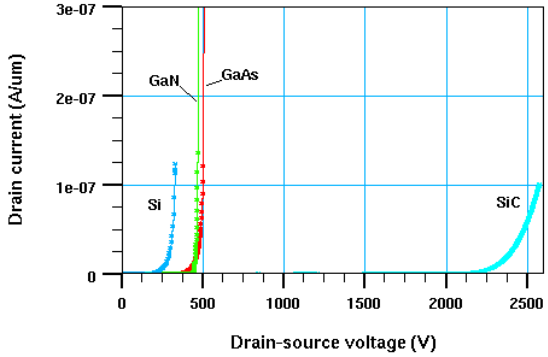

Figure 7. Comparison of predicted hold-off voltages for the Si, GaAs, SiC, and GaN devices. The plot for the GaN JFET was obtained at Vgs= -25V.

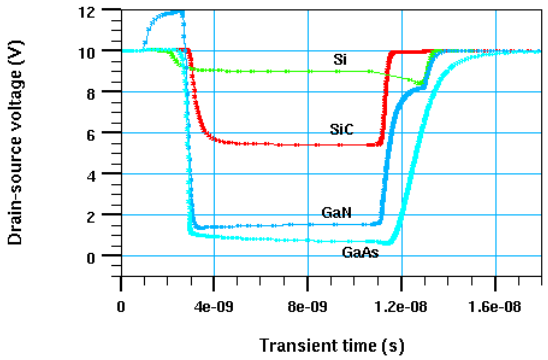

Figure 8. Comparison of predicted switching performances of the Si, SiC, GaN and GaAs devices.

Figures 7 and 8 show our simulation results for the hold-off voltages and switching performances of JFET's based on the four materials. No material has the best results for both characteristics. The 4H-SiC JFET has the best breakdown voltage, while the GaAs and GaN JFET's have faster switching speeds. As mentioned above, GaN has the highest theoretical figures of merit. Our simulations have shown that, unlike the other materials, the GaN JFET is a normally on device. A negative gate bias is needed to obtain a hold-off voltage for this device. Figure 9 shows the predicted influence of gate bias on the hold-off voltage of the GaN JFET. The reasons for this

effect are unknown. The lowest carrier concentration in the drift region is of the order of 10^{16} cm^{-3}. In Ref. [17], Bunea et al. have pointed out that this is due to self-heating effects.

In addition, as can be seen in Figure 10, the high thermal conductivity of SiC causes it to have the lowest temperature increase at conduction, which is favorable for high power applications.

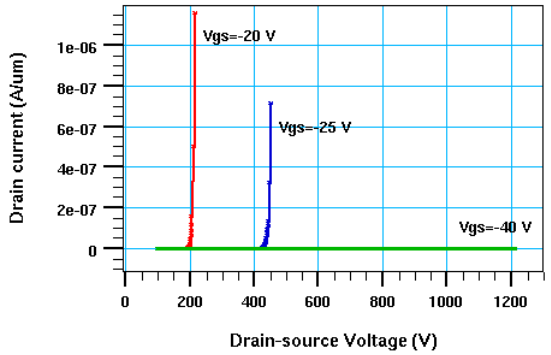

Figure 9. Predicted effect of gate bias on the hold-off voltage of the GaN JFET.

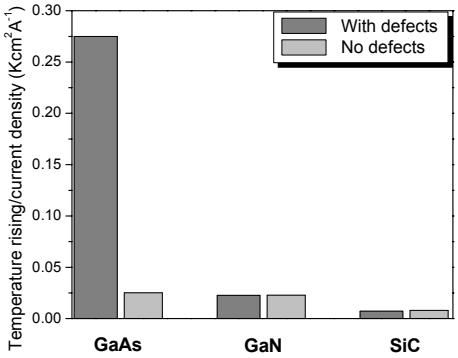

Figure 10. Ratio between temperature rising and current density for GaAs, GaN and SiC JFET's.

V. SUMMARY

We have performed a 2-dimensional device simulation study of a JFET structure using Si, SiC, GaAs, and GaN as the materials used in the device. Deep level defects as well as perfect Si, GaAs, 4H-SiC and Wurtzite GaN have been included in the study. The effect of defects on electrical properties was discussed. Our results show that, of the materials we have considered, 4H-SiC is the most promising for pulsed power applications based on our simulations and on the available data.

VI. REFERENCES

[1] T. P. Chow and R. Tyagi, "Wide Bandgap Compound Semiconductors for Superior High-Voltage Unipolar Power Devices," IEEE Trans. Electron Devices **41**, 1481-1483, 1994.

[2] Sang-Kwon Lee, "Processing and Characterization of Silicon Carbide (6H- and 4H-SiC) Contacts for High Power and High Temperature Device Applications," Ph.D. Dissertation, Department of Microelectronics and Information Technology, KTH, Royal Institute of Technology, 2002.

[3] ATLAS®, Silvaco International, CA, USA.

[4] M. Levinshtein, S. Rumyantsev and M. Shur, "Properties of Advanced Semiconductor Materials," United Kingdom: John Wiley & Sons, 2001.

[5]NSM Archive, http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaAs/index.html

[6] B. J. Baliga, "Modern Power Devices," New York: John Wiley & Sons, 1987.

[7] X. Gu, C. Myles, A Kuthi, Q. Shui and M. Gundersen, "Gallium Arsenide and Silicon FET-type Switches for Repetitive Pulsed Power Applications," in Proc. of 25th International Powre Modulator Symposium, 2002, p. 437.

[8] S. T. Pantelides, "Deep Centers in Semiconductors," New York: Gordon and Breach Science Publishers, 1985.

[9] S. Schwetlick, W. Seifert, R. Pickenhain and R. Schwabe, "Reduced EL2 Concentration in MOCVD GaAs by Addition of NH_3 During Growth," J. Crystal Growth **96**, 378-382, 1989.

[10]M. Rogalla, Th. Eich, N. Evans, R. Geppert, R. Goppert, R. Irsigler, J. Ludwig, K. Runge, Th. Schmid and D. G. Marder, "Analysis of Trapping and Detrapping in Semi-insulating GaAs Detectors," Nuclear Instruments and Methods in Phys. Res. A **395**, 49-53, 1997.

[11]S. Mitra, M.V. Rao, K. Jones, N. Papanicolaou and S. Wilson, "Deep levels in ion implanted field effect transistors on SiC," Solid-State Elec. **47**, 193-198, 2003.

[12]A. A. Lebedev, "Deep level centers in silicon carbide: A review," Semiconductors **33**, 107-129, 1999.

[13]J. Pankove and T. Doustakas, "Gallium Nitride (GaN) II," Semiconductors and Semimetals **57**, San Diego: Academic Press, 1999.

[14]M. Manasreh, D. Fischer and W. Mitchel, "The EL2 defect in GaAs: some recent developments," Phys. Stat. Sol. (b) **154**, 11-41, 1989.

[15]D. McGregor, R. Rojeski and G. Knoll, "Evidence for field enhanced electron capture by EL2 centers in semi-insulating GaAs and the effect on GaAs radiation detectors," J. Appl. Phys. **75**, 7910-7915, 1994.

[16]G. Bunea, S. Dunham and T. Moustakas, "Modeling of a GaN based static induction transistor," MRS Internet J. Nitride Semicond. Res. **4S1**, G6.41, 1999.

[17]N. Weimann, L. Eastman, D. Doppalapudi, H. Ng and T.D. Moustakas, "Scattering of electrons at threading dislocations in GaN," J. Appl. Phys. **83**, 3656-3659, 1998.

[18]Q. Shui, X. Gu, M. Mazzola, M .Gundersen and C. Myles "Simulations of a high power 4H-SiC JFET and its GaAs counterpart," will present at 14th International Pulsed Power Conference, June 16-18, 2003, Dallax TX.