GALLIUM ARSENIDE AND SILICON FET-TYPE SWITCHES FOR REPETITIVE PULSED POWER APPLICATIONS*

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Abstract

Repetitive pulsed-power generators with nanosecond rise times and multi-kilovolt outputs commonly employ silicon MOSFET switches. Gallium arsenide FET switches hold the promise of faster operation, higher voltage hold-off, and greater current densities. The realization of this promise requires an understanding of the physical and practical limits of Si- and GaAs-based devices. In this paper, the results of ATLAS simulations on a Si MOSFET and on a GaAs SIT are presented. The results show that GaAs-based devices are superior to those based on Si in terms of switching speeds and power dissipation, but that they have a relatively higher leakage current.

I. INTRODUCTION

In pulsed generators, the performance of switches can be an important factor that affects the power efficiency, the pulse shape and the repetition rate of pulses. With long life-time and integrating ability, Si Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET's) are commonly used in multi-kilovolt, hundred amperes pulse systems for fast switching speeds (< 50 ns) [1]. However, Si power MOSFET's have low current rise rates due to the small electron mobility and the narrow energy band gap of Si. In addition, many high-voltage systems require series stacking of switches to reach needed voltages. Because of these effects, it is worthwhile to consider both the limitations of synchronous triggering, and the long-term reliability of the trigger circuit during fast switching transients [2].

Other materials, with wider energy band gaps and larger electron mobilities, such as GaAs, SiC, and diamond have been developed for high-power applications. Among these, GaAs is a good candidate due to its high electron mobility [3] (8500 $cm^2/V{\cdot}s$) and relatively mature processing technology. The physical nature of GaAs also promises a higher hold-off voltage capability and a higher operating temperature, in comparison with Si-based switches. Also, since GaAs is a direct band gap material, the devices based on it have optoelectronic capability, which can result in simple triggering circuits and low-jitter operation. Hadizad *et al.* [1] have found, both theoretically and experimentally, that FET's based on GaAs will dissipate less power than those based on Si. However, GaAs-based FET's have also shown certain fundamental limitations [4].

In this paper, we review some of the practical and physical limitations of Si- and GaAs-based FET switches and present the results of simulations on a Si MOSFET and on a GaAs SIT.

II. DEVICE LIMITATIONS

A. Practical Difficulties

It is very difficult to fabricate GaAs-based devices with the purity of typical Si-based devices. The presence of a large concentration of native defects in GaAs, such as EL2 and EL2*, strongly affects the electrical properties of GaAs-based devices. These defects can be scattering centers and their induced energy levels in the gap can trap electrons. As a result, the observed electron mobility is much less than the theoretical value, about 4000 $cm^2/V{\cdot}s$ for semi-insulating GaAs.

At 300 K, the thermal conductivity for GaAs is about 0.46 watts/cm·C°, one third of that for Si [3]. Thermal runaway thus can become a serious issue in designing GaAs power switches for high voltage, high current applications.

B. "Lock-on" Effect in GaAs

The "lock-on" effect is a high gain, high field switching mechanism that has been observed in devices fabricated with semi-insulating GaAs and InP [5], but it has not been observed in Si [6]. This effect has been observed with both optical and electronic switch triggering. The lock-on electric field for a given material is independent of the initial bias and of the switch geometry. For GaAs, this field is in the range of ~ 3.5 - 9.5 kV/cm [6]. A detailed discussion of this phenomenon, including experimental data, may be found in reference [7]. This effect causes high forward drop and high power dissipation for bulk

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switches based on GaAs [6]. Also, it is always accompanied by current filaments [8], which can result in local device and contact damage and thus to a reduced switch lifetime.

A number of models have been proposed to explain the "lock-on" effect, including metastable impact ionization of deep EL2 traps [9]; a combination of double injection, trap filling and avalanche breakdown [10], [11]; and avalanche injection by a transferred electron effect (Gunn effect) [6]. Recently, Hjalmarson *et al.* have developed a collective impact ionization theory to explain the "lock-on" effect in semi-insulating GaAs [12]. The basic idea of this theory is that, at high carrier density ($n > 10^{17} cm^{-3}$), carrier-carrier scattering leads to a significant increase in the impact ionization probability. This leads to a collective breakdown, which occurs at a much lower field (the lock-on field) than the bulk breakdown field of GaAs.

III. DEVICE SIMULATIONS

In order to compare GaAs- and Si-based switching devices, we have used the ATLAS simulation software to study a vertical Si MOSFET and a recessed gate GaAs Static Induction Transistor (SIT).

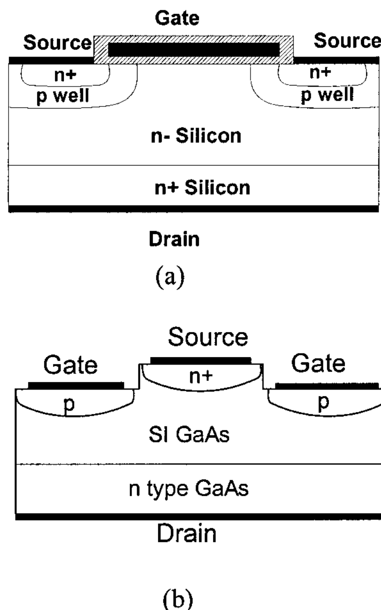

Figure 1. Cross sectional structure of the switch devices considered here: (a) Si MOSFET and (b) GaAs SIT.

A. Device Structure Description

Figure 1 shows a schematic of the cross sectional structures of the Si MOSFET and the GaAs SIT which we have considered. To hold off high voltage, each device has a 30 μm epi-layer as the drift region. The n^+ drain regions are doped at $n = 3.5\times10^{18}$ cm^{-3} to form ohmic contacts. In the GaAs SIT, the p-n junction under the gate is reverse-biased, which introduces a channel potential barrier for electrons under the source. When the gate is triggered by the application of a positive voltage pulse, the p-n junction depletion layer decreases and the channel potential barrier disappears. Electrons are emitted from the source, which is at ground potential, and are accelerated to the drain. To be realistic, a deep donor energy level (0.65eV below the conduction band minimum [13]), with a defect concentration of (1.6310^{16} cm^{-3}) was included in the GaAs SIT simulations.

B. Simulation Results

In the ATLAS simulations, we have extracted the specific on-resistance versus blocking voltage for both the Si- and the GaAs-based devices. These are 25.4 $m\Omega\cdot cm^2$ and 64.2 $m\Omega\cdot cm^2$, respectively. Figure 2 shows a plot containing our results and the results of others for the specific on-resistance versus blocking voltage in the devices considered here. In that figure, the square and the triangle symbols are experimental results on a GaAs SIT [14] and experimental results on a Si MOSFET [15], while the diamond and the star symbols are the ATLAS simulation results for the GaAs SIT and for the Si MOSFET of Fig. 1. The solid lines in Fig. 2 show the theoretical limits for these Si and GaAs –based devices.

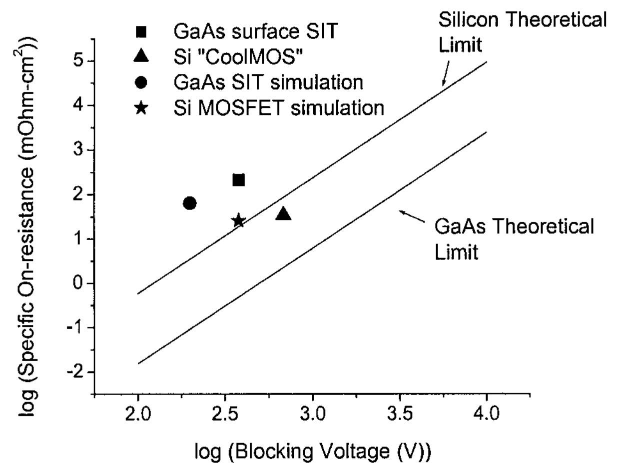

Figure 2. Theoretical and experimental specific on-resistance, as a function of blocking voltage for GaAs and Si-based switching devices.

Figure 3 shows our ATLAS simulation results for the drain source current versus drain source voltage of the GaAs SIT and Si MOSFET devices of Fig. 1. From Fig. 3, the hold-off voltage properties of these devices can be obtained. As may be seen in the figure, these voltages are about 370 V for the GaAs SIT and 350 V for the Si MOSFET. For the same drift layer thickness, the GaAs SIT yielded a higher leakage current. This might be an effect of the native defects included in the simulations. In Ref. [14], surface GaAs SIT's with drift layer lengths of 15 μm were fabricated and had a drain-source hold-off voltage of ~ 200 V. Since the hold-off voltage is roughly

proportional to the length of the drift region [16], the 370 V obtained in our simulations is about right.

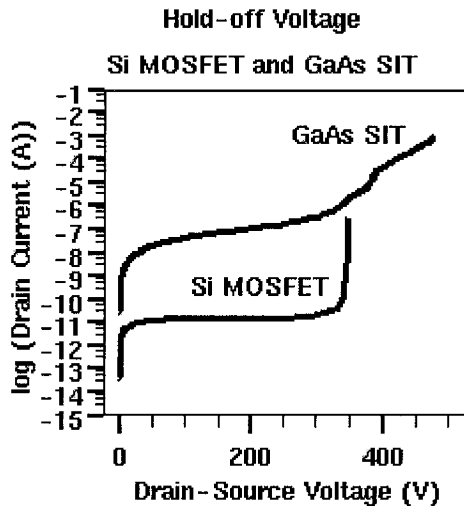

Figure 3. Simulation results for drain source current versus drain source voltage for the Si MOSFET and the GaAs SIT considered here. From this figure, the hold-off voltages of the devices can be obtained.

Our ATLAS simulation results for the switching performances of the two devices we have considered are shown in Fig. 4. In that figure, the drain source voltage is plotted as a function of time. In the simulations, the source was connected to ground. The drain resistor was 500 kΩ, which was connected to a 100 V voltage source. The triggering pulse at the gate had a 2 ns rise time, a 2 ns fall time, and an 8 ns pulse length. As is shown in the plot, the forward voltage drop on the GaAs SIT is much less than that on the Si MOSFET. Also, the SIT gives a fast turn on / turn off capability. These results are consistent with previous theoretical and experimental discussions [1, 4, 17].

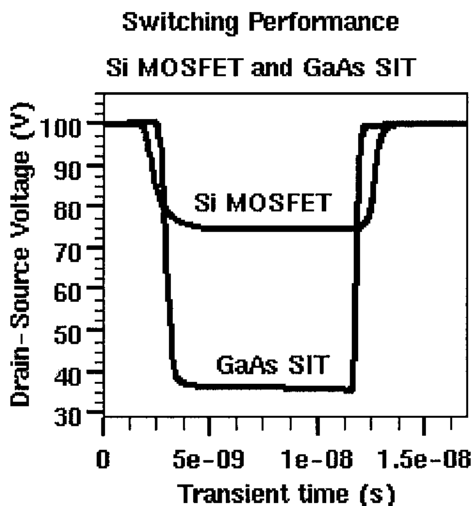

Figure 4. Switching properties of the Si MOSFET and the GaAs SIT considered here.

IV. SUMMARY

Using the ATLAS simulation package, we have made a comparison of GaAs SIT and Si MOSFET-type switches for pulsed power applications. Our simulation results show that, due to the higher electron mobility and larger energy band gap of GaAs, the GaAs-based FET has a faster switching speed and greater power efficiency than the Si MOSFET. However, the leakage current of the GaAs-based FET is higher than that of the Si MOSFET.

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